REMARKS

Claims 53-76 remain in the present application. Claims 53, 62 and 71 are amended herein. Applicants respectfully submit that no new matter has been added as a result of the claim amendments. Applicants respectfully request further examination and reconsideration of the rejections.

Claim Rejections – 35 U.S.C. §103

Claims 53-76 are rejected under 35 U.S.C. §103(a) as being unpatentable over United States Patent Number 3,805,247 to Zucker et al. (referred to herein as "Zucker") in view of United States Patent Number 5,949,982 to Frankeny et al. (referred to herein as "Frankeny") and further in view of United States Patent Number 5,394,551 to Holt et al. (referred to herein as "Holt"). Applicants respectfully submit that the embodiments of the present invention as recited in Claims 53-76 are not rendered obvious by Zucker in view of Frankeny and further in view of Holt for the following reasons.

Applicants respectfully direct the Examiner to independent Claim 53 which recites a system comprising (emphasis added):

> a plurality of memory resources;
> a plurality of peripheral resources;
> a plurality of processors;
> a memory controller coupled to said plurality of processors and said plurality of memory resources, wherein said memory controller comprises a first resource controller operable to control access by said plurality of processors to said plurality of memory resources using a hardware semaphore unit, wherein said first resource controller is further operable to implement respective buses for coupling said plurality of processors to said plurality of memory resources, wherein said memory controller is further operable to enable each processor of said plurality of processors to simultaneously access a respective portion of a memory resource of said

plurality of memory resources, and wherein said memory controller is further operable to enable each of said plurality of processors to have priority access to a respective instruction memory of a plurality of instruction memories; and

a peripheral controller coupled to said plurality of processors and said plurality of peripheral resources, wherein said peripheral controller comprises a second resource controller operable to control access by said plurality of processors to said plurality of peripheral resources using said hardware semaphore unit, and wherein said second resource controller is further operable to implement respective buses for coupling said plurality of processors to said plurality of peripheral resources.

Independent Claims 62 and 71 recite elements similar to independent Claim 53. Claims 54-61, 63-70 and 72-76 depend from their respective independent Claims and recite further elements of the claimed invention.

Applicants respectfully submit that Zucker fails to teach or suggest the elements of "wherein said memory controller is further operable to enable each of said plurality of processors to have priority access to a respective instruction memory of a plurality of instruction memories" as recited in independent Claim 53. As described in the present application, a memory controller is operable to enable each of a plurality of processors to have priority access to a respective instruction memory of a plurality of instruction memories. Support for the claim amendments can be found in, for example, lines 11-14 of page 9 of the instant specification.

In contrast to the claimed embodiments, Applicants fail to find any teaching or suggestion in Zucker of a memory controller which enables each of said plurality of processors to have priority access to a respective instruction memory of a plurality of instruction memories as claimed. Accordingly,

Applicants reiterate that Zucker fails to teach or suggest the elements of "wherein said memory controller is further operable to enable each of said plurality of processors to have priority access to a respective instruction memory of a plurality of instruction memories" as recited in independent Claim 53.

Applicants respectfully submit that Frankeny and/or Holt, either alone or in combination with Zucker, fails to cure the deficiencies of Zucker discussed herein. More specifically, Applicants respectfully submit that Frankeny and/or Holt, either alone or in combination with Zucker, also fails to teach or suggest the elements of "wherein said memory controller is further operable to enable each of said plurality of processors to have priority access to a respective instruction memory of a plurality of instruction memories" as recited in independent Claim 53.

For these reasons, Applicants respectfully submit that independent Claim 53 is not rendered obvious by Zucker in view of Frankeny and further in view of Holt. Since independent Claims 62 and 71 recite elements similar to those discussed above with respect to independent Claim 53, Applicants respectfully submit that independent Claims 62 and 71 are not rendered obvious by Zucker in view of Frankeny and further in view of Holt. Since Claims 54-61, 63-70 and 72-76 recite further elements of the invention claimed in their respective independent Claims, Applicants respectfully submit that Claims 54-61, 63-70 and 72-76 are also not rendered obvious by Zucker in view of Frankeny and further in

view of Holt. Thus, Applicants respectfully submit that Claims 53-76 overcome the 35 U.S.C. §103(a) rejection of record, and therefore, are allowable.

CONCLUSION

Applicants respectfully submit that Claims 53-76 are in condition for allowance and Applicants earnestly solicit such action from the Examiner.

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,

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Dated: 12 / 2 / 2010 /BMF/

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